[*720,750*] which can configured to operate in synchronism with at least the first address-strobing signal [*1043*].--

-- ~~67~~ 66 (New) The FPGA device of Claim ~~45~~ 44 and further comprising:

(d) a plurality of programmably configurable input/output blocks (IOB's) [*700*] coupled to the CLB interconnect resources and having configurable I/O storage means [*720,750*] which can configured to operate in synchronism with said one or more data-strobing signals [*1058,1059,1093*].--

Remarks

The above Amendments and these Remarks are in reply to the Office action mailed 07/05/00.

Summary of Status of Pending Claims (and of Other Issues)

Claims 1-21 were pending in this case at the time of the latest Office action.

> > Each of **Claims 1-21** was rejected under 35 U.S.C. **§102(e)** as being fully anticipated by McGowan U.S. Pat. No. 5,744,980; issued 04/28/98, filed 2/16/96.

> > Also cited but not applied was Cliff U.S. Pat. No. 5,828,229 (issued 10/27/98 and based on a chain of continuations and CIP's whose filings end 11/08/95 and stretch back to 05/08/92).

> > Claims 1, 3 were rejected for indefiniteness.

> > The specification was objected to.

Summary of Present Response

Claim 20 is withdrawn.

Claims 1-5, 8-19, 21 are amended.

Claims 22-67 are newly introduced.

The Specification is amended.

Overview of Advantages of Claimed Subject Matter

The present application is directed to synchronization of address capture, memory read, and/or memory write operations within an FPGA array having embedded memory blocks.

In one embodiment represented by Fig. 9, it is seen that address signals 872 and 874 may be synchronously captured in response to ADRCLK signal 933 while data signals for respective ports 903 and 904 may be independently captured in response to separate port clocks RWCLK (931) and ROCLK (932). Under this embodiment, new addresses may be supplied and locally captured for writing or reading of next data even as previously output data (READ data) is being still output by the READ output registers 972 and 962 of respective Port-1 and Port-2 and being used by logic blocks of the FPGA. In other words, address and data transfers may be pipelined.

In Fig. 11A, box 1101, it is seen that address-validation may occur at a first time point time point t_1 while data-validation may occur at a different, second time point time point t_2. (The text for items 1121 and 1171 at specification page 106, line 12 explains that Fig. 11A shows t_2 following t_1 merely for sake of example.) One reason why address-validation may occur at a different time than data-validation is because the address and data signals may travel along different paths of the configurable interconnect.

Using box 1101 of Fig. 11A as an example, address signals from source 1120 may have to travel through a longer path and thus incur longer delay because they travel

through both of HIC 1152 (Horizontal Interconnect Channel) and SVIC 1160 (Special Interconnect Channel). On the other hand, data signals from source 1170 may be able to travel through a shorter path (HIC 1150) and thus incur a comparatively shorter delay. The timings for the respective address-capture and data-capture functions may be advantageously varied according to circumstances so that bus time is not wasted while data signals wait for address signals to catch up to them or vice versa.

In application Fig. 10, the independent timing of respective address-capture and data-capture functions may be provided respectively by the ADRCLK1 signal on line 1015 and by the RWCLK1 signal supplied to Din register 10R1 and Dout register 10R2. Such independent strobing of address-capture and data-capture functions allows for a more efficient, pipelined usage of signal-conveying interconnect (see items 1057 and 1058 of Fig. 10) within the FPGA because either or both of Port-1 and Port-2 can output retrieved and register-captured data even as next address signals are being captured by their respective address registers 1011 and 1012.

It will be shown that the art of record does not provide for independent strobing of address-capture and data-capture functions while also solving the memory-controls "congestion" problem (see McGowan col. 2, lines 56-65 and also col. 7, lines 7-15). Other aspects of the here claimed subject matter will become apparent in the below discussions.

Initial Comparison with applied McGowan reference

In rejecting Claim 1, the outstanding Office Action at page 4, line 10, equates each of McGowan's memory segments 16-1, 16-2, etc. with a corresponding one of the memory blocks that are recited in the claim to be embedded within a respective one of rows of logic units. Applicant respectfully traverses this reading of McGowan. It will be

later shown that McGowan teaches away from the idea of separately and independently capturing address and data signals.

Support for Amendment to Claim 1

Claim 1 is amended to clarify that "each said logic unit can internally process its respective second plurality of input logic bits without using said horizontal interconnect channels or other general interconnect for such internal processing".

Applicant agrees that there is no ipsis verbis (word-for-word identical) support for this clarifying language in the specification. However, there are several things which inherently support the introduction of this language. It is not new matter and it is amply supported by the specification as originally filed.

First, there is the ordinary and customary understanding that those of skill in the relevant art have as to what is intended by a "unit" that is of the type, "logic unit". There is also the ordinary and customary understanding of skilled practitioners as to what is intended by a "module" that is of the type, "logic function module". (The latter phrase appears in the McGowan reference.)

One lay dictionary defines "unit" as being, among other possibilities, "a single thing, person or group that is a constituent of a group" and as "a piece or complex of apparatus serving to perform one particular function" (Webster's Ninth New Collegiate Dictionary, 1990). The same lay dictionary defines "module" as being, among other possibilities, "an independently-operable **unit** that is part of a total structure [such as] of a space vehicle" {emphasis and bracketed text added}. In view of this, the ordinary artisan would see a rough, one-to-one correspondence between what McGowan calls a "logic function module" (12) and what in Claim 1 is recited as a "logic unit". That same understanding guides away

from seeing correspondence between an *arbitrarily* selected group of McGowan's "logic function modules" (12) and what in Claim 1 is recited as a "logic unit".

A second factor to be considered is that the present specification distinguishes between general interconnect and CLB's. It is explained at page 5, lines 3-etc. that an FPGA device can be characterized as having four major features including: (4) An interconnect network that is provided for carrying signal traffic within the FPGA device *between* various CLB's and/or *between* various IOB's and/or *between* various IOB's and CLB's [emphasis added]. The word, "between" guides away from interpreting general interconnect as being an internal part of a CLB or an equivalent. Note specification page 6, lines 14-17 which allows for calling of the repeated units that carry out user-programmed logic functions by alternate names.

A third factor to be considered is that the present specification describes "wedged-together" VGB's as being such that vertical and horizontal interconnect channels (VIC's and HIC's) do not cut through a mirror-wise opposed congregation of VGB's (a super-VGB). See specification page 43, lines 5-13. This explicitly demonstrates that each VGB and/or super-VGB can internally process its respective input signals without using horizontal interconnect channels or other general interconnect for such internal processing. Thus the proposed clarifying language for Claim 1 is fully supported at least by this passage.

Support for "independently-usable" as added to Claim 1

With respect to this phrase, again there is no ipsis verbis (word-for-word identical) support for this clarifying language in the specification. However, page 26, lines 7-11 state "in one embodiment, each of memory blocks, ML0-ML7 and MR0-MR7 has an internal SRAM array organized as a group of 32 nibbles (32x4 = 128 bits) where each nibble is individually addressable by five address bits". This is a clear indication that each

SRAM block is independently usable as a memory block. When this aspect is combined with the detailed discussions concerning the transmission of independent address and control signals along the SVIC (special vertical interconnect channel --see item 860 of Fig. 8 for example) it becomes abundantly clear that the SRAM blocks described in the present specification are independently-usable as such (each as an independent SRAM block).

The memory "segments" 16-1, 16-2, etc. of McGowan clearly do not qualify as independently-usable memory blocks. See for example, McGowan col. 7, lines 23-25 ("distribute components of the SRAM block among ... portions 16-1 [through] 16-4" -- emphasis added).

Applicant's Analysis of Evidence in Record

As part of the evidentiary record, it is necessary to obtain an understanding of the scope of the prior art (as seen without hindsight through the eyes of the ordinary artisan at the relevant time) and to correctly construe the claims (in light of what the ordinary artisan reasonably sees in view of the specification). McGowan 5,744,980 forms the foundation under 35 USC §102(e) for all art-based rejections. Thus an analysis of the McGowan document is presented first.

Reservation of Right to Challenge McGowan as a §102(e) reference

A document does not become a valid reference under 35 USC §102(e) {as applicable to applications filed before 11/29/00} simply because the PTO published it. All the detailed requirements of §102(e) must be met. Applicant reserves here the right to challenge McGowan as being a valid §102(e) reference should the need arise. Nothing said herein constitutes an acquiescence by Applicant that McGowan is a valid §102(e)

reference. For one thing, it is noted that McGowan stresses the distributed nature of the address inputs and control inputs and data inputs as such are programmably connectable to adjacent interconnect lines. Yet McGowan Fig. 2 shows no specific pattern of such programmable connections to specific interconnect lines. And at col. 8, lines 14-21 as well as elsewhere McGowan readily admits that such specific patterns for the preferred embodiment are intentionally not shown. This raises a question concerning the adequacy of McGowan's disclosure pursuant to 35 USC §112. If the §112 requirements are not met, then §102(e) is also not met.

Applicant's Interpretation of the McGowan '980 reference

McGowan is directed to the provision of on-chip SRAM in FPGA devices. See col. 1, line 35.

According to McGowan's teachings, each SRAM block (16) "spans" a plural number of rows of logic function modules (12). Indeed, in the example of Fig. 2, one SRAM block is denoted by the dashed boundary 16 as being comprised of four "segments", 16-1 through 16-4, and this one SRAM block spans across the rows occupied by logic function modules 12-1, 12-2, 12-3 and 12-4. See col. 4, lines 32-35.

Further according to McGowan, the inputs and outputs of each SRAM block (16) are "distributed" or "spread" amongst five routing channels so as to avoid congestion and mimic the general routing density of the rest of the FPGA chip. See col. 5, lines 13-16 and also col. 7, lines 13-16. These distributed "inputs" of the one SRAM block (16) include address, control, and data inputs (col. 5, lines 29-39).

Additionally according to McGowan, data that is read from memory moves from the multi-rows-spanning SRAM block (16) to a neighboring logic function module (12) by being output onto a vertical, 4-channels spanning wire (e.g., the vertical output wire of driver 5

in segment 16-2 of Fig. 2). The output data signal then routes through a switchbox such as represented by the left 'X' on wire 18-2c of Fig. 2 for propagation onto a desired one of plural horizontal interconnect channels such as routing channel 18-2 or 18-1 and for pick up by a channel-neighboring logic function module (12). In the example of Fig. 2, logic function module 12-5 pick ups the signal via the right 'X' on wire 18-2c. This example is detailed at McGowan col. 6, lines 9-28.

Claim 1 Distinguished over McGowan

The outstanding grounds of rejection assert that each of boxes 16-1, 16-2, etc. in McGowan Fig. 2 is synonymous with one of the (independently-usable) memory blocks recited in Claim 1. (Claim 1 is amended to clarify that each of the memory blocks is independently-usable.)

It is seen from the above, detailed analysis of McGowan that this finding of fact within the Office action (page 4, line 10) is in error. Each of boxes 16-1, 16-2, etc. is not an independently-usable memory block, but rather a distributed "segment" of a multi-rows-spanning, but unitary SRAM block 16. McGowan teaches away from the idea of providing each independently-usable memory block as being embedded within one of the rows of logic units. Thus, it is respectfully submitted that a recission of the outstanding rejection is in order in view of this misunderstanding of the facts.

Essentially same arguments were presented and accepted by the US PTO in earlier filed Ser. No. 08/996,049 --now US Pat 6,127,843 issued 10/3/00--. So that begs the question, what is it about the present claims that is different?

The answer is that the present claims are directed to address and data synchronization aspects such as detailed in Fig. 10 of the present application.

Defects and Details of McGowan Re-visited

With respect to its address and data synchronization aspects, the McGowan document has special problems which were not earlier pointed out in the prosecution of Ser. No. 08/996,049; but which Applicant now wishes to highlight.

In McGowan Fig. 3, note there is an unreferenced line extending upwardly from WRITE LOGIC 38 into boxes 34, 22, 28 and 26. At col. 7, line 66- col. 8, line 1 it is explained that the following signals are all synchronized to the WCLK (write clock): Write input data (WD) on bus 30, write address data (WRAD) on bus 36, and miscellaneous control signals WEN 44, BLKEN 42. What this means is that the timing of the write input data (WD) is not independent from the timing of the write address data (WRAD). McGowan asserts in one place (col. 7, lines 19-25) that the "optimal" embodiment distributes components across the segments in a "linear ... manner". However, at another place (col. 8, lines 13-21) McGowan states that inputs to WRITE LOGIC 38 are connectable to "a wiring channel" without specifying more. At yet at another place (col. 9, lines 57-65) McGowan states that inputs to READ LOGIC 66 are connectable to "a wiring channel" without specifying more. Nothing is said about how the WRAD, WD, RDAD and RD lines are connected to adjacent wiring channels except that at col. 7, lines 13-15 it is stated that the additional address lines (supposedly WRAD and RDAD) are compensated for by "spreading" SRAM inputs over several routing channels. How that squares with the concentration of WRITE LOGIC inputs and READ LOGIC inputs into respective wiring channels is left unknown. And there lies a problem with the McGowan document serving as a viable 102(e) reference.

Analysis of Cliff '229

Figs. 20-21 show a "RAM-LAB" (col. 16, line 40-etc.). Input data, address and control signals are acquired from Global-H lines 220 by way of partially-populated box 424 and an "intra-LAB" bus 414 (col. 16, line 60-etc.). Bus 414 is seen in Fig. 21-1 as coupling to data-input register 430 (col. 17, line 53) and to address-input register 438 (col. 17, line 58). In Fig. 21-2, data-output register 454 (col. 19, line 66) couples to global H bus 220 and to global V bus 222. Each of registers 430, 438 and 454 is clocked by register clock 478 emanating from control 446 (col. 18, line 35, col. 19, line 58).

Cliff '229 does not teach or suggest the concept of having independent address-strobing and data-strobing clocks.

Claim 1 Distinguished over Cliff '229

Claim 1 is amended to recite each first address-capturing register as being clockable by a first address-strobing signal that is independent of the first data-strobing signal. Cliff '229 teaches away by calling for a common register clock 478.

Analysis of Young WO 98/10517

Applicant's Information Disclosure Statement of March 2000, citing Young WO 98/10517 has been initialed by the Examiner. Nevertheless further review of Young is provided here.

Fig. 2 shows details of a single "RAM block". This RAM block, which is also shown coarsely in Fig. 1B, has four general interconnect, horizontal buses L0-L3 passing through a bottom portion of the block. Each of buses L0-L3 corresponds to a "row" of logic blocks. In Fig. 2, it is seen that the dual ports include read-output data lines DOA-0:8 and DOB-0:8 (page 8, line 24); as well as write-input data lines DIA-0:8 and DIB-0:8. Separate

address buses ADA-0:8 and ADB-0:8 service these RW ports A and B and "pentagon connections" (see Fig. 4A) provide couplings to the vertical conductors of buses of DIN-A, DIN-B, ADDR-A, ADDR-B (see page 8, line 29). The illustrated RAM block also has CLK-A and CLK-B terminals. Although the clock terminals are mentioned several times throughout the Young WO 98/10517 document, there does not appear to be any description of the specific functions of these. Thus it is left to speculation what they do. It does not appear that Young WO 98/10517 teaches or suggests the idea of independently clocking address and data signals however because only one clock (CLKA) is provided for all the functions of port A and only one clock (CLKB) is provided for all the functions of port B.

Claim 1 Distinguished over Young 10517

Claim 1 is amended to recite each first address-capturing register as being clockable by a first address-strobing signal that is independent of the first data-strobing signal. Young appears to teach away by showing a single clock terminal for both address and data buses of a given RAM port (A or B).

Claims 3-9 Distinguished over McGowan

With respect to **Claims 3-4**, the outstanding grounds of rejection appear to assert that McGowan teaches data width matching wherein each addressable set of storage data bits that includes at least P3 bits (e.g., 4 bits) is transferable by way of a corresponding HIC to or from its corresponding row of P4 logic units, where the P3 plurality of bits correspond to the P3 plurality of output logic bits (e.g., 4 bits) that are producible by each logic unit. Applicant respectfully disagrees.

It is correct to state generally, that each multi-rows-spanning SRAM block 16 of McGowan can input 4 or 8 bits of data through its write port (28) and can output 4 or 8

bits of data through its read port (62). But there is no factual basis for asserting that such nibbles (4 bits) or bytes (8 bits) are transferable by way of a specific horizontal interconnect channel to and/or from a corresponding row of logic units (12). McGowan is silent on this point.

McGowan is also essentially silent about the specific configuration of the logic units (12). At col. 3, lines 41-46, McGowan states that the logic function modules (12) may be ***any*** one of a variety of circuits, these not being limited to the examples provided at lines 41-46. Thus McGowan is at least silent with respect to the matching of the bit width of the logic function modules with the bit width of the embedded SRAM blocks. It is fair to say that McGowan in fact teaches away from such bit width matching because of McGowan's statement that "**any**" logic function module design will do.

With respect to **Claim 5**, the above-provided clarification regarding the meaning of "wedged together" is fully supported by application page 43, line 10-etc. McGowan's teaching of a multi-rows-spanning SRAM block 16 is clearly away from the subject matter of Claim 5.

With respect to **Claim 6**, the outstanding grounds of rejection rely on the items denoted as "18-n" in McGowan Fig. 3. It is respectfully submitted that this reliance is misplaced in view of the above, detailed analysis of McGowan. It has been demonstrated that McGowan explicitly admits a failure to disclose the specific manner in which address and/or control and/or data signals are routed to the multi-rows-spanning SRAM block 16. See again, McGowan col. 8, lines 14-21. McGowan Fig. 2 does not show more than a generic coupling of the input amplifiers 1-4 of segment 16-4 of SRAM block 16 to respective lines a-d of horizontal interconnect channel 18-5. There is no teaching or remote suggestion that an embedded memory subsystem should include at least one special interconnect channel for supplying address signals to a respective set of memory blocks.

With respect to **Claim 7**, the same comments apply as to Claim 6. The outstanding grounds of rejection rely on general interconnect items "18-n" in McGowan Fig. 3. These do not represent a special interconnect channel that belongs to an embedded memory subsystem.

With respect to **Claim 8**, the outstanding grounds of rejection rely on output line drivers 5 and 6 such as those shown in box 16-1 of McGowan Fig. 2 for constituting equivalents to the recited first and second data ports.

It is respectfully submitted that such an equivalence is not reasonable in view of the descriptions of data ports as are supplied in the specification and even in the body of Claim 8. The claim itself requires that each memory block have at least first and second address ports each for receiving address signals identifying the storage data to be output by a *corresponding one* of the at least first and second data ports. The claim itself requires a capability by way of which independent address signals may be respectively carried for application to respective ones of the first and second address ports.

It would be correct to assert that McGowan Fig. 3 shows two independently-addressable data ports, namely, the **write-only** port defined by latches 28 and the **read-only** port defined by latches 62. But these two ports do not qualify as each being for "**outputting** storage data" per Claim 8. Moreover, there is absolutely nothing in the McGowan disclosure that can reasonably qualify as first and second address-carrying components of a special interconnect channel. Thus, it is respectfully submitted that a prima facie case of anticipation or obviousness has not been made out.

With respect to **Claim 9**, it is again respectfully submitted that the foundational facts being relied upon are misplaced in view of the above, detailed analysis of McGowan. It has been demonstrated that McGowan explicitly admits a failure to disclose the specific manner in which control signals are routed to the SRAM block 16. There is no teaching or

remote suggestion in McGowan that an embedded memory subsystem should include at least one special interconnect channel for supplying control signals to a respective set of memory blocks.

Claim 10 Distinguished over McGowan

With respect to Claim 10, the outstanding grounds of rejection merely parrot the language of the claim and point vaguely at input buffers 1-4 of McGowan Fig. 2. It should now be apparent from the above analysis of McGowan that the reference fails to teach both a read/write data port and a read-only data port. Each multi-rows-spanning SRAM block 16 of McGowan Fig. 3 has one **write-only** data port (28) and one **read-only** data port (62). An anticipation rejection requires a showing that each and every limitation of the claim is fully met by one reference. McGowan fails to even meet that portion of Claim 10 (as amended above) that calls for at least two readable data ports. Moreover, there is no evidence that McGowan teaches or suggests the further concepts of Claim 10 concerning each data port being connectable by user-configurable intercouplings to long-haul interconnect lines.

Claim 14 Distinguished over McGowan

With respect to Claim 14, no grounds of rejection are articulated in the outstanding Office action. Instead it is assumed that all of Claims 11-13, 14-21 recite essentially the same things as set forth in Claims 1-10. It is respectfully submitted that this is not the case.

Claim 14 is supported by application Fig. 10 and its corresponding text. It is seen in Fig. 10 and explained in the specification (page 87, lines 9-etc.) that an address-strobing signal can originate as ADRCLK0 in clock source 1055. An interconnect-delayed version

of this signal may be seen as ADRCLK1 on the clock input of address-capturing register 1011 (or alternatively ADRCLK0 and ADRCLK1 may be an essentially same Global clock signal as is explained in the specification). Another interconnect-delayed version of this address-timing signal, which is delayed at least as much as ADRCLK1 is, may be seen as ADRCLK3 on the horizontal or vertical interconnect line (H/V IC) 1001 that connects to clock-acquisition logic 1021 in the upper left corner of the drawing. See also specification page 90, lines 6-etc. If an appropriate configuration is established, the next address signal (NEW ADDR2 1027) cannot pass through flip-flop 1022 and CSEQ section 1023 to become next address signal 1024 until address-capturing register 1011 has assuredly captured the old version of address signal 1024.

McGowan does not teach such a method for assuring that an old address signal is captured before a next address signal is output onto the interconnect. The read-clock (RCLK 72) and read address signal (RDAD 52) of McGowan are merely assumed to be valid at a same time in Fig. 3 thereof.

Cliff '229 is also silent with respect to the operation of the sources of register clock 478 (Fig. 21-1) and the read or write address signals. For Fig. 26 thereof, Cliff '229 merely describes box 1028 (see col. 26, line 8) as programmable logic and lines 1030a,b as sub-buses. There appears to be no discussion of clock timing.

Young '10517 is similarly silent with respect to the operation of the CLKA and CLKB terminals shown in Fig. 2.

Support for Claims 15-16

At specification page 90, lines 24-etc. it is explained that the source of an old address signal 1024 can include CSEQ portion 1023 (Fig. 10) where the latter corresponds to multiplexers 668, 620 and driver 630 of Fig. 6B. These elements inherently provide a

delay for the loop that feeds the ADRCLK3 signal to the FF portion 10222 and the CSEQ portion 1023 when the latter provide a next address signal for output on line 1024. At specification page 90, lines 5-etc. it is explained that CSE register 1022 corresponds in one embodiment to 667 of Fig. 6B. It may be seen from these that either one or both of the steps of outputting the old/next address and coupling the first address-strobing signal through delaying logic may include passing respective signals through CSEQ part 1023 and/or flip-flop 1022. Logic 1021 may provide yet further delay for the ADRCLK3 signal. Thus the capture of an old address signal in register 1011 may be assured to occur before CSEQ section 1023 outputs a next address signal. The art of record does not teach or suggest such steps.

Comments re Claims 19-20

Claim 20 is withdrawn and Claim 19 is amended to recite among other things: "(c) defining a third route through said interconnect resources from the address clock sourcing circuit to an address-changing circuit ....." and "(d) defining a fourth route through said interconnect resources from a read clock sourcing circuit of the FPGA device to the at least one registered data output port."

The art of record does not teach or suggest the concept of having independent address-strobing and data-strobing paths. Although Fig. 2 of McGowan '980 does not show it, col. 10, lines 4-etc. imply that RCLK 72 is coupled via an inverter to read latches 54. In Cliff '229 at Fig. 21-1 thereof, a same register clock 478 is shared by address register 438 and data register 430. As explained above, Young 10517 is silent about the uses of the CLKA and CLKB signals in Fig. 2 thereof.

Comments re Claim 21

The outstanding grounds of rejection assume that Claim 21 is essentially similar in scope to others of the claims. Applicant respectfully disagrees and submits that a prima facie case of anticipation or obviousness has not been made out. The art of record does not teach or suggest a method for producing configuration signals for configuring an FPGA device in a manner which encourages the creation in the configured FPGA of a shared signal route that transmits an address-strobing clock signal to a registered address input port and that transmits an address-change allowing signal to one or more address-sourcing modules and that transmits a data-strobing signal to one or more registered data output ports as is recited in part (c) of Claim 21.

Summarized Arguments

The present application discloses a unique FPGA architecture in which embedded memory is conformably meshed with configurable logic units (e.g., VGB's) and configurable interconnect (e.g., HIC's, VIC's and switchboxes) so as to allow for simplified synchronization of address and/or data capture and transmission of new address and data signals.

The specification contains extensive descriptions of Fig. 10 and how the various structures represented thereby may be used to provide affirmative handshaking between capture of first address and/or data signals and outputting of next address and/or data signals. The art of record (McGowan '980, Cliff '229, and Young 10517) does not appear to address the problem of how to provide such pipelined operations within an FPGA and does not teach or suggest the subject matter defined by the pending claims.

In view of the above Amendments and Remarks, reconsideration of Claims 1-19, 20 is requested and consideration of newly added Claims 22-67 is requested.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including November 5, 2000.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: October 24, 2000

By: _____

Gideon Gimlan
Reg. No. 31,955
(408) 748-7300

FLIESLER, DUBB, MEYER & LOVEJOY LLP
Four Embarcadero Center, Suite 400
San Francisco, California 94111-4156
Telephone: (415) 362-3800

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